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EXAMINER

LAI, VINCENT

ART UNIT	PAPER NUMBER
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2181

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,932	SCHULZ ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.


Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/7/2006

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-22 have been examined.

Response to Amendment

2. Acknowledgement is made of amendments to the title, specification, drawings, and claims.
3. Objections to the title and specifications are withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-3, 5-10, and 15-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Disclosure of a pipeline circuit being operable simultaneously and asynchronously relative to other pipeline circuits could not be found in the specification of the patent application. It is not obvious or apparent to the examiner as how figures 4 and 6 convey a pipeline circuit being operable simultaneously and asynchronously relative to other pipeline circuits. By having a sync signal, it would seem the opposite is true and that the pipeline circuits run

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synchronously. These new features are claimed in the amended claims 1 and 15.

Claims 2-3, 5-10, and 16-22 are rejected for their dependencies on claims 1 or 15.

5. Claims 1-3, 5-10, and 15-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is unclear as how an asynchronous circuit can exist when a synchronization signal is present (see figures 4 and 6), as these two would seemingly contradict each other.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al (US Pat. No. 6,282,627; herein referred to as "Wong").

As per claim 4, Wong discloses *a pipeline accelerator, comprising: a communication bus* [see Wong, Fig. 6, element 609; Col. 5, lines 24-26]; *and a plurality*

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of pipeline units each coupled to the communication bus [see Wong, Fig. 3, element "Datapath Slice"; Col. 5, lines 30-34] and each comprising a respective hardwired-pipeline circuit [see Wong, Fig. 6, elements "DPU"; Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping...")].

Wong does not explicitly disclose each of the hardwired-pipeline circuits is disposed on a respective field-programmable gate array.

However, Wong does disclose the hardwired-pipeline circuits being disposed on a reconfigurable "course-grained silicon implementation" (Col. 5, line 36). Furthermore, Wong discloses the use of FPGAs for the same utility (Col. 5, line 37) and furthermore discloses the disadvantages of utilizing an FPGA (Col. 5, lines 37-38). Furthermore, Wong discloses the point that FPGA implementations are more flexible (Col. 1, lines 51-52) and were not used within the invention due to the preferred nature of courser-grained silicon for long bit width arithmetic function modules (Col. 5, lines 39-40). The advantage, disclosed by Wong, of utilizing FPGAs for a hardwired-pipeline circuit would therefore have been to include a higher level of flexibility. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize an FPGA as a hardwired-pipeline circuit in place of the courser-grained silicon if a higher degree of flexibility was needed without heed to long bit arithmetic function modules.

7. Claims 1-3, 5-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Ebeling et al (U.S. Patent # 6,023,742), herein referred to as Ebeling.

As per claim 1, Wong discloses *a pipeline accelerator, comprising: a communication bus* [see Wong, Fig. 6, element 609; Col. 5, lines 24-26]; *and a plurality of pipeline units each coupled to the communication bus* [see Wong, Fig. 3, element "Datapath Slice"; Col. 5, lines 30-34] *and each comprising a respective hardwired-pipeline circuit* [see Wong, Fig. 6, elements "DPU"; Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping...")].

Wong does not explicitly disclose being operable simultaneously with and asynchronously relative to at least one of the other hardwired-pipeline circuits.

Ebeling does disclose a datapath that operates parallel (See column 13, lines 9-10) and asynchronously (See column 9, lines 62-64).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Wong with Ebeling because both inventions deal with reconfigurable data paths with emphasis for flexibility (See abstracts of both patents) and thus if one or more features belonging to a similar invention were desirable, it would be obvious to combine those features into the invention.

As per claim 2, Wong discloses *the pipeline accelerator of claim 1 wherein each of the pipeline units comprises: a respective memory coupled to the hardwired-pipeline circuit* [see Wong, Fig. 7, element LSM; Col. 4, lines 28-31]; *and wherein the hardwired-pipeline circuit is operable to, receive data from the communication bus* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *load the data into the memory* [see Wong, Col. 9, lines 2-4 ("loading coprocessor registers")], *retrieve the data from the memory* [see

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Wong, Col. 4, lines 55-57; Examiner's note: Wong discloses data passing from a register (within the ACM/LSM fabric) to a DPU ("cloud"), thus Wong discloses reading data from a memory coupled to a hardwire-pipeline circuit.], *process the retrieved data* [see Wong, Fig. 5, element 503; Examiner's note: Wong discloses a "cloud" of reconfigurable logic which processes data sent from the previously cited register.], *and drive the processed data onto the communication bus* [see Wong, Col. 9, lines 4-7; Examiner's note: Wong discloses results being sent back to the main processor, which would have utilized the communication bus.].

As per claim 3, Wong discloses *the pipeline accelerator of claim 1 wherein each of the pipeline units comprises: a respective memory coupled to the hardwired-pipeline circuit* [see Wong, Fig. 7, element LSM]; *and wherein the hardwired-pipeline circuit is operable to, receive data from the communication bus* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *process the data* [see Wong, Fig. 5, element 503; Examiner's note: Wong discloses a "cloud" of reconfigurable logic which processes data sent from the previously cited register.], *load the processed data into the memory* [see Wong, Col. 4, lines 55-57; Examiner's note: In the cited sections, Wong discloses a circular movement of data, however it is apparent upon reading the specification that the flow of data is not necessarily in a circular motion (Col. 9, lines 47-50). This allows a serial connection of datapath elements such as combinational logic to a register and then returned to processor. Due to the reconfigurable nature of the ACM it is impractical to list or summarize all possible function configurations, therefore, the previously described

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configuration is considered to be of merit by the examiner.], *retrieve the processed data from the memory, and load the processed data onto the communication bus* [see Wong, Col. 9, lines 4-7; Examiner's note: Wong discloses results being sent back to the main processor, which would have utilized the communication bus and would also retrieve the values from a stored location within the ACM.].

As per claim 5, Wong discloses *the pipeline accelerator of claim 1, further comprising: a pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a corresponding datapath slice through a bus.]; *and a pipeline-bus interface coupled to the communication bus and to the pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24].

As per claim 6, Wong discloses *the pipeline accelerator of claim 1, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus **609** and elements **610a,b**], *a respective branch coupled to each pipeline unit* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *and a router coupled to each of the branches* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28) thus routing functions to individual pipeline units.].

As per claim 7, Wong discloses *the pipeline accelerator of claim 1, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b], *a respective branch* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b] *coupled to each pipeline unit* [see Wong, Fig. 6, element 610a,b]; *a router coupled to each of the branches* [s see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28) thus routing functions to individual pipeline units.]; *a pipeline bus* [see Wong, Fig. 3, elements 319a,b; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a corresponding datapath slice via a bus]; *and a pipeline-bus interface coupled to the router and to the pipeline bus* [see Wong, Fig. 3, elements 319a,b].

As per claim 8, Wong discloses *the communication bus [comprising] a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus **609** and elements **610a,b**], *a respective branch coupled to each pipeline unit; a router coupled to each of the branches* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *a pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a

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corresponding datapath slice.]; *a pipeline-bus interface coupled to the router and to the pipeline bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24].

Wong does not explicitly disclose *a secondary bus coupled to the router*.

However, Wong does disclose the use of a MAC controller (Fig. 3, element 304), which is commonly used to access a network. However, Wong does not explicitly disclose how the MAC controller interfaces with the ACM within the disclosure. Given the state of the art at the time of invention, it would have been known that vector processors are well suited for handling large quantities of raw data and a mechanism for routing data directly to the pipeline units would have been advantageous. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to assume that the MAC controller disclosed by Wong would have been coupled to the router disclosed by Wong with the intention of facilitating the transmission of raw data for processing.

As per claim 9, Wong discloses *the pipeline accelerator of claim 1 wherein: the communication bus is operable to receive data addressed to one of the pipeline units* [see Wong, Col. 9, lines 2-4]; *and the one pipeline circuit is operable to accept the data; and the other pipeline circuits are operable to reject the data* [see Wong, Col. 10, lines 7-10; lines 37-45; Examiner's note: Wong uses the function map table (Fig. 18a) to and the block configuration words (Fig. 18b) to correctly allow the corresponding pipeline unit to process the data and the other pipeline units to reject processing of the data.].

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As per claim 10, Wong discloses *the pipeline accelerator of claim 1, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b], *a respective branch coupled to each pipeline unit* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *a router coupled to each of the branches* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28)] *and operable to, receive data addressed to one of the pipeline units* [see Wong, Col. 9, lines 2-4; Examiner's note: Applicant is reminded of the method disclosed by Wong to identify a receiving pipeline unit as describe with regard to claim 9 of this application.], *and provide the data to the one pipeline unit via the respective branch of the communication bus* [Examiner's note: It is clear that data sent to a particular pipeline would be required to utilize the branch bus disclosed by Wong in Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b].

As per claim 11, Wong discloses *a computing machine, comprising: a processor* [see Wong, Fig. 3, element 302]; *a pipeline bus coupled to the processor* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24; Examiner's note: It would have been obvious to one of ordinary skill in the art at the time of invention that the bus interfaces would have been coupled to the CPU and to a corresponding datapath slice via a bus] *and operable to carry data and hardwired-pipeline-configuration information* [see Wong, Fig. 3, elements 320, 311, and 302; Examiner's note: Please see 'Response to

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Arguments' below]; *and a pipeline accelerator comprising, a communication bus* [see Wong, Fig. 6, element 609; Col. 5, lines 24-26], *a pipeline-bus interface coupled between the pipeline bus and the communication bus* [see Wong, Fig. 3, elements 319a,b; Col. 4, lines 22-24], *and a plurality of pipeline units each coupled to the communication bus* [see Wong, Fig. 3, element "Datapath Slice"; Col. 5, lines 30-34] *and each comprising a respective hardwired-pipeline circuit* [see Wong, Fig. 6, elements "DPU"; Col. 5, lines 12-15. ("The DPUs provide the data path functionality for the behavioral mapping...")].

As per claim 12, Wong discloses *the computing machine of claim 11 wherein: the processor is operable to generate a message that identifies one of the pipeline units* [see Wong, Col. 9, lines 2-4 (instruction to turn control over to ACM); Col. 10, line 37 (a load instruction to specify which plane of DPUs to load)] *and to drive the message onto the pipeline bus* [Examiner's note: It is inherent with respect to Figure 3, that data is transferred between the CPU and ACM via a bus and bus interfaces]; *the pipeline-bus interface is operable to couple the message to the communication bus* [see Wong, Fig. 3, element 319a; Examiner's note: It would have been known at the time of invention that an interface is utilized to couple messages between busses]; *the pipeline units are each operable to analyze the message* [see Wong, Col. 10, lines 37-46; Examiner's note: Block configuration words are used to validate the message received, that is, to validate that the pipeline unit is the correct unit to receive the message.]; *the identified pipeline unit is operable to accept the message; and the other pipeline circuits are*

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operable to reject the message [see Wong, Col. 10, lines 7-10; lines 37-45; Examiner's note: Wong uses the function map table (Fig. 18a) to and the block configuration words (Fig. 18b) to correctly allow the corresponding pipeline unit to process the data and the other pipeline units to reject processing of the data.].

As per claim 13, Wong discloses *the computing machine of claim 11, further comprising: wherein the communication bus comprises a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b], *a respective branch* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b] *coupled to each pipeline unit* [see Wong, Fig. 6, element 610a,b]; *wherein the processor is operable to generate a message that identifies one of the pipeline units* [see Wong, Col. 9, lines 2-4 (instruction to turn control over to ACM); Col. 10, line 37 (a load instruction to specify which plane of DPUs to load)] *and to drive the message onto the pipeline bus* [Examiner's note: It is inherent with respect to Figure 3, that data is transferred between the CPU and ACM via a bus and bus interfaces]; *and a router coupled to each of the branches and to the pipeline-bus interface* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28)] *and operable to receive the message from the pipeline-bus interface and to provide the message to the identified pipeline unit* [see Wong, Col. 5, lines 22-28; Examiner's note: Wong discloses the BLU receiving messages from the communication bus and thus the interface and configuring the datapath accordingly, thus providing the message.].

As per claim 14, Wong discloses *the communication bus* [comprising] *a plurality of branches* [see Wong, Fig. 6, double-arrowed busses between communication bus 609 and elements 610a,b], *a respective branch coupled to each pipeline unit* [see Wong, Fig. 6, coupling of double sided arrow to 610a/620a]; *and a router coupled to each of the branches* [see Wong, Fig. 6, element 611a,b; Examiner's note: elements 611a/b determine the interconnect if any between DPUs (Col. 5, lines 26-28) thus routing functions to individual pipeline units.] [and] *to the pipeline bus interface* [see Wong, Fig. 3, elements 319a,b].

Wong does not explicitly disclose *a secondary bus and a router coupled to the secondary bus*.

However, Wong does disclose the use of a MAC controller (Fig. 3, element 304), which is commonly used to access a network. However, Wong does not explicitly disclose how the MAC controller interfaces with the ACM within the disclosure. Given the state of the art at the time of invention, it would have been known that vector processors are well suited for handling large quantities of raw data and a mechanism for routing data directly to the pipeline units would have been advantageous. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to assume that the MAC controller disclosed by Wong would have been coupled to the router disclosed by Wong with the intention of facilitating the transmission of raw data for processing.

As per claim 15, Wong discloses *a method, comprising: sending data to first of a plurality of pipeline units via a communication bus* [see Wong, Col. 9, lines 2-4; Examiner's note: Wong discloses sending data to the coprocessor registers, it would have been inherent that upon configuration, a hardwired pipeline would require a starting position for processing data.], *each pipeline unit including a respective hardwired pipeline* [see Wong, Fig. 6, element 621a et al. ("DPU" elements); Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping...")]; *and processing the data with the first pipeline unit* [see Wong, Col. 9, lines 4-7; Examiner's note: In this cite, Wong discloses an overall process, it is inherent that this overall process would contain processing of a first pipeline unit.].

Wong does not disclose processing the second data with the second pipeline unit asynchronously with respect to the first pipeline unit and while the first pipeline unit is processing the first data.

Ebeling does disclose a datapath that operates parallel (See column 13, lines 9-10) and asynchronously (See column 9, lines 62-64).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Wong with Ebeling because both inventions deal with reconfigurable data paths with emphasis for flexibility (See abstracts of both patents) and thus if one or more features belonging to a similar invention were desirable, it would be obvious to combine those features into the invention.

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As per claim 16, Wong discloses *the method of claim 15 wherein sending the data comprises: sending the data to a router* [see Wong, Col. 5, lines 22-24; Examiner's note: Data is sent from the CPU to the BLU.]; *and providing the first data to the first pipeline unit with the router via a respective first branch of the communication bus* [see Wong, Col. 5, lines 26-28; Examiner's note: Bus 609 in Fig. 6 allows transfer of both control and data to BLU 610a. BLU 610a controls the configuration of DPUs in pipeline unit 620a and transfers data through the bus located between the BLU and DPUs as shown in Fig. 6].

As per claim 17, Wong discloses *the method of claim 15 wherein sending the data comprises sending the first data to the first pipeline unit with a processor* [see Wong, Col. 6, lines 2-4].

As per claim 18, Wong discloses *the method of claim 15 wherein sending the data comprises sending the first data to the first pipeline with a second of the plurality of pipeline units* [see Wong, Fig. 6, elements 630a; Col. 9, lines 47-50; Examiner's note: Wong discloses an inter-block communication bus (likened to buses connecting pipeline units in Fig. 8 of the applicant) that enables blocks to send data to each other. Given the multi-block function disclosed by Wong in Col. 9, it would have been obvious that a second unit could send data to a first unit via the inter-block bus.].

As per claim 19, Wong discloses *the method of claim 15, further comprising driving the processed first data onto the communication bus with the first pipeline unit* [see Wong, Col. 5, lines 24-26; Examiner's note: Bus 609 allows for bidirectional transfer of data from the ACM to the CPU. It would have been apparent that after data has finished processing it would have been steered back to the processor via Bus 609 (Col. 9, lines 4-7)].

As per claim 20, Wong discloses *the method of claim 15 wherein processing the first data with the first pipeline unit comprises: receiving the first data from the communication bus with a hardwired-pipeline circuit* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *loading the first data into a memory with the hardwired-pipeline circuit* [see Wong, Col. 9, lines 2-4], *retrieving the first data from the memory with the hardwired-pipeline circuit* [see Wong, Col. 4, lines 55-57; Examiner's note: Wong discloses data passing from a register (within the ACM/LSM fabric) to a DPU ("cloud"), thus Wong discloses reading data from a memory coupled to a hardwire-pipeline circuit.], *and processing the retrieved first data with the hardwired-pipeline circuit* [see Wong, Fig. 5, element 503].

As per claim 21, Wong discloses *the method of claim 15 wherein processing the first data with the first pipeline unit comprises: receiving the first data from the communication bus with a hardwired-pipeline circuit* [see Wong, Fig. 6/7, element 609; Col. 5, lines 24-26], *processing the received first data with the hardwired-pipeline circuit*

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[see Wong, Fig. 5, element 503], *and loading the processed first data into a memory with the hardwired-pipeline circuit* [see Wong, Col. 9, lines 2-4], *and retrieving the processed first data from the memory with the hardwired-pipeline circuit* [see Wong, Col. 4, lines 55-57; Examiner's note: Wong discloses data passing from a register (within the ACM/LSM fabric) to a DPU ("cloud"), thus Wong discloses reading data from a memory coupled to a hardwire-pipeline circuit.], *and driving the processed first data onto the communication bus with the hardwired-pipeline circuit* [see Wong, Col. 9, lines 4-7; Examiner's note: Wong discloses results being sent back to the main processor, which would have utilized the communication bus].

As per claim 22, Wong discloses *the method of claim 15, further comprising: generating a message that includes the first data and that identifies the first pipeline unit as a recipient of the message* [see Wong, Col. 9, line 45; Examiner's note: Wong discloses a load instruction which specifies which block a function is to reside in.]; *and wherein sending the first data to the first pipeline unit comprises determining from the message that the first pipeline is a recipient of the message* [see Wong, Col. 10, lines 7-10; lines 37-45; Examiner's note: Wong uses the function map table (Fig. 18a) to and the block configuration words (Fig. 18b) to correctly allow the corresponding pipeline unit to process the data and the other pipeline units to reject processing of the data.].

As per claim 23, Wong discloses a computing machine, comprising: a memory operable to store program instructions (See figure 3, LSM array and SDRAM: Both are

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connected to buses that can fetch instructions and thus can store program instructions); a program-instruction bus coupled to memory (See figure 3: The bus instruction fetch buses are program-instruction buses); a pipeline bus that is separate from the program-instruction bus (See figure 3: Memory instruction fetch bus, a pipeline bus, is different from the normal instruction fetch bus); a processor (See figure 3, CPU 302) coupled to the program-instruction bus and to the pipeline bus (See figure 3: All buses lead to the processor); the pipeline accelerator comprising, a communication bus (See Fig. 6, element 609; Col. 5, lines 24-26); a pipeline-bus interface coupled to the communication bus and to the pipeline bus (See fig. 3, elements 319a,b; col. 4, lines 22-24); and a plurality of pipeline units each coupled to the communication bus (See fig. 3, element "Datapath Slice"; Col. 5, lines 30-34) and each comprising a respective hardwired-pipeline circuit (See fig. 6, elements "DPU"; Col. 5, lines 12-15 ("The DPUs provide the data path functionality for the behavioral mapping..."))).

Wong does not teach a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

Ebeling does disclose a pipeline accelerator inoperable to communicate directly with the program-instruction bus (See figure 8: The data path and instruction converge at one point).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Wong with Ebeling because both inventions deal with reconfigurable data paths with emphasis for flexibility (See abstracts of both

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patents) and thus if one or more features belonging to a similar invention were desirable, it would be obvious to combine those features into the invention.

As per claim 24, Wong discloses a method, comprising: retrieving with a processor program instructions from a memory via a program-instruction bus (See figure 3: Memory instruction fetch and SDRAM instruction fetch is possible); executing the instructions with the processors (See figure 3: Done inherently with processor); and transferring information between the processor and pipeline units of a pipeline accelerator via a pipeline bus that is separate from the program-instruction bus (See figure 3: More than one type of bus is present).

Wong does not teach a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

Ebeling does disclose a pipeline accelerator inoperable to communicate directly with the program-instruction bus (See figure 8: The data path and instruction converge at one point).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Wong with Ebeling because both inventions deal with reconfigurable data paths with emphasis for flexibility (See abstracts of both patents) and thus if one or more features belonging to a similar invention were desirable, it would be obvious to combine those features into the invention.

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As per claim 25, Wong discloses wherein the information comprises data (Information is inherently data); wherein transferring the information comprises sending the data from the processor to the pipeline units (See figure 16: ACM can receive data from ALU); and processing the data with the pipeline units (See figure 16: ACM is connected to ALU).

As per claim 26, Wong discloses wherein the information comprises data (Information is inherently data); wherein transferring the information comprises sending the data from the pipeline units to the processor (See figure 16: ACM can receive data from ALU); and processing the data with the processor (See figure 16: ACM is connected to ALU).

As per claim 27, Wong discloses wherein the information comprises addresses of the pipeline units (See column 7, line 63- column 8, line 2).

Response to Arguments

8. Applicant's arguments filed on 21 June 2006 have been fully considered but they are not persuasive.

Arguments pertaining to claims 1 (and subsequently 2-3, 5-7, and 9-10 are addressed above), 15 (and subsequently 16-22), and 23-27 are addressed above.

As per claim 4, Wong teaches the FPGA implementation as the invention is meant to be an improvement upon using FPGA technology. In doing so, Wong discloses the use of FPGAs in the system and even admits flexibility as an attractive quality of FPGAs (See column 1, lines 52-54).

Examiner also cannot find alleged assertion that examiner stated it would be obvious to scale Wong's single-chip architecture to a multi-chip architecture in previous office action; however, examiner does agree with statement. It would have been obvious to a person having ordinary skill in the art at the time the invention was made that scaling down is more complicated than scaling up and therefore a system that utilizes separate chips would be an easier system to implement. Examiner would like to point to MPEP 2144.04, part IV: Changes in size, shape, or sequence of adding ingredients. Changes in size/proportion do not constitute patentability; *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.) Since scaling is deemed unpatentable, it must mean that scaling would be obvious to one having ordinary skill in the art at the time the invention was made. Please note cited MPEP 2144.04 also establishes rearrangement of parts (part VI.C) and making separable are not grounds (part V.C) for patentability and thus such actions would be deemed obvious.

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As per claim 11, acknowledgement and agreement is made to the applicant's attorney's admission that "one of more other busses carry configuration data from the Local Store Memory (LSM)." Examiner would like to point to figure 3 in which the LSM array is connected to the processor through a memory bus, being one of the other busses, and thus would be able to carry data and hardwired-pipeline-configuration information.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

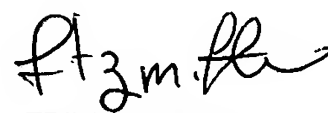
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

vi
July 25, 2006


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8/7/2006